

Figure 1A

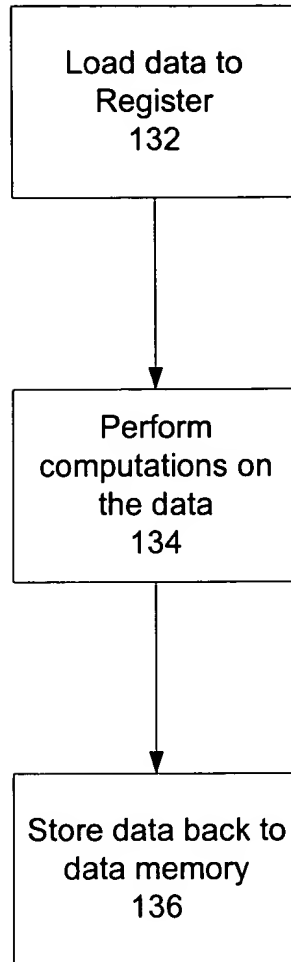


Figure 1B

0988295-05204  
2022-5628860

OPCode 6 bits	Source1 Register 5 bits	Source2 Register 5 bits	Target Register 5 bits	Sub-OPCode 11 bits
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Figure 1C

OPCode 6 bits	Target Register 5 bits	Source1 Register 5 bits	Immediate 16 bits
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Figure 1D

0988297.062901

200

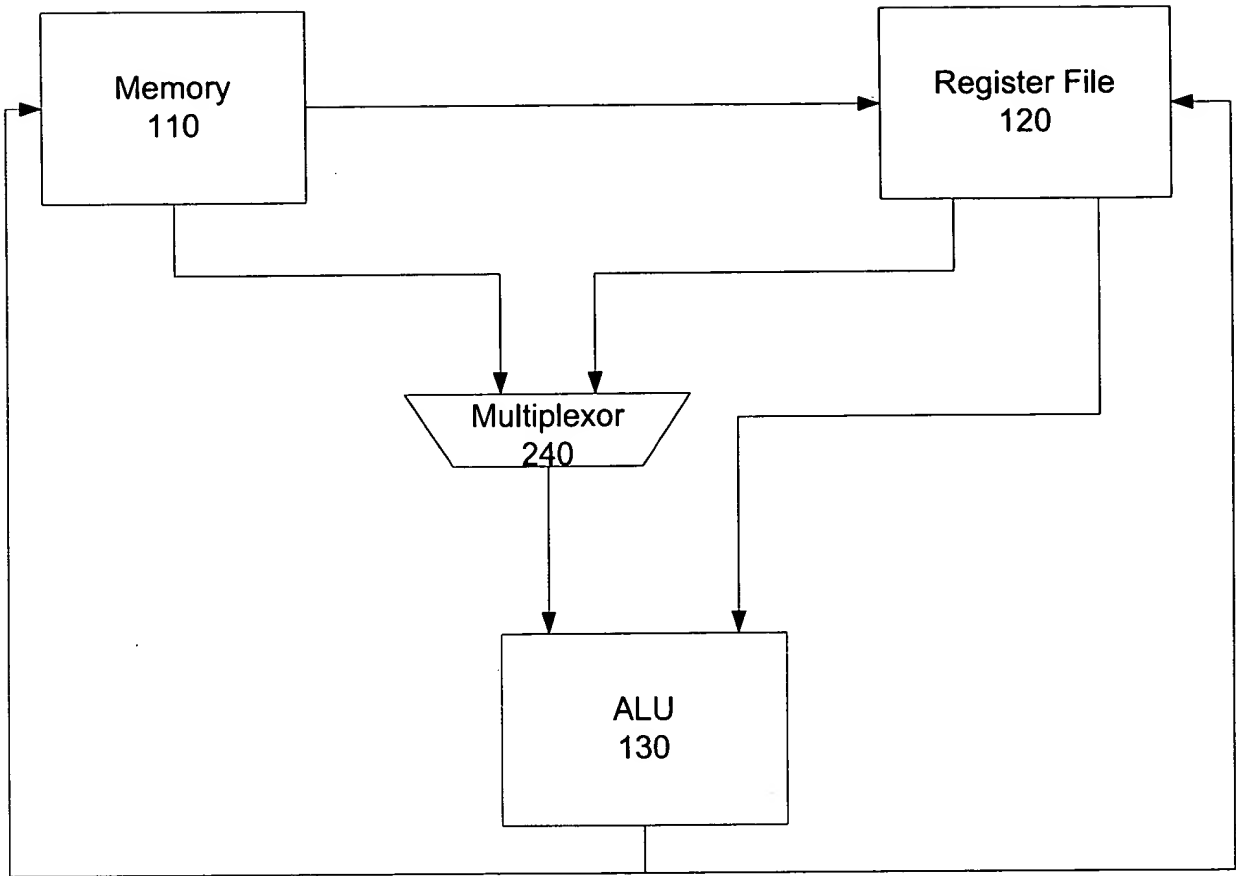


Figure 2

300

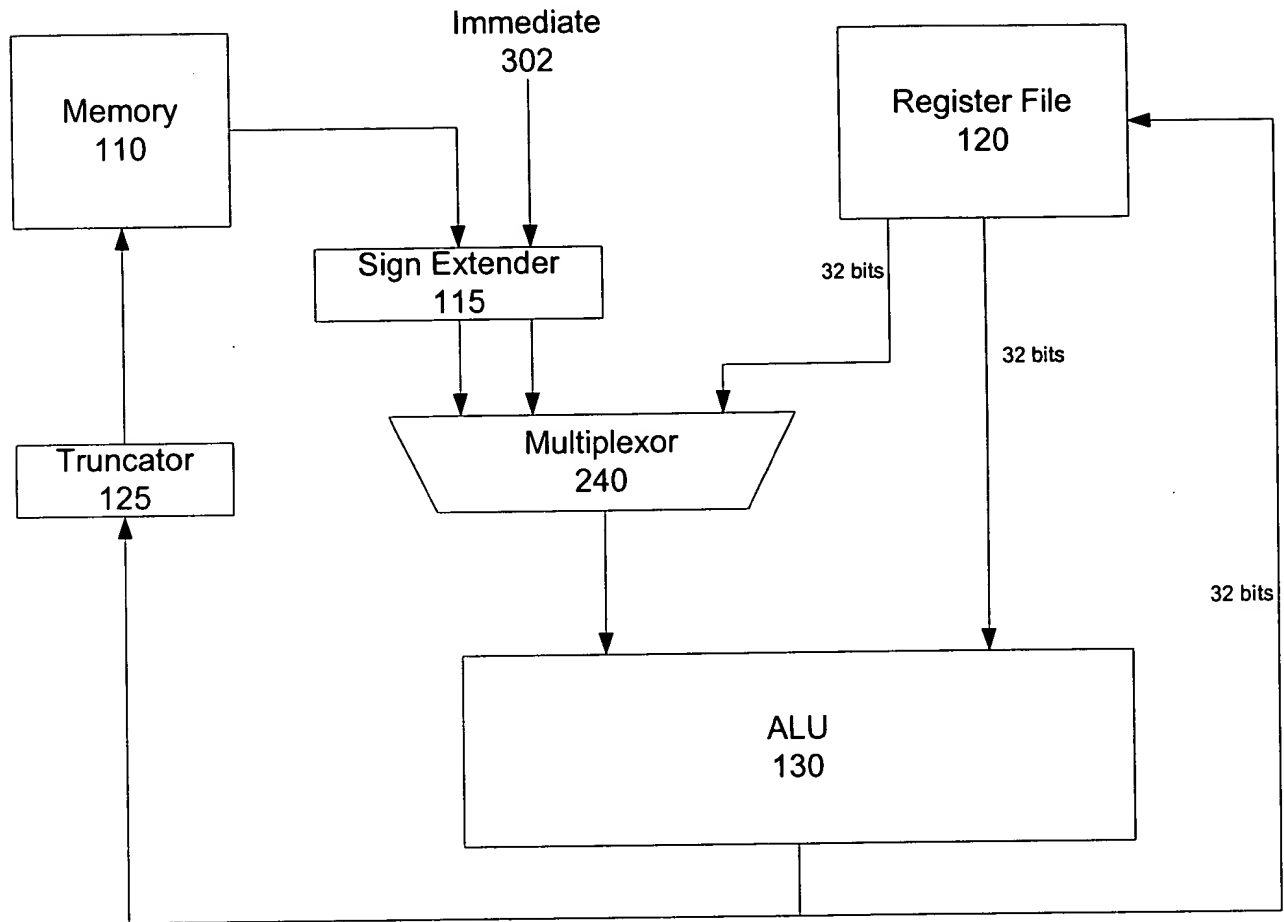


Figure 3A

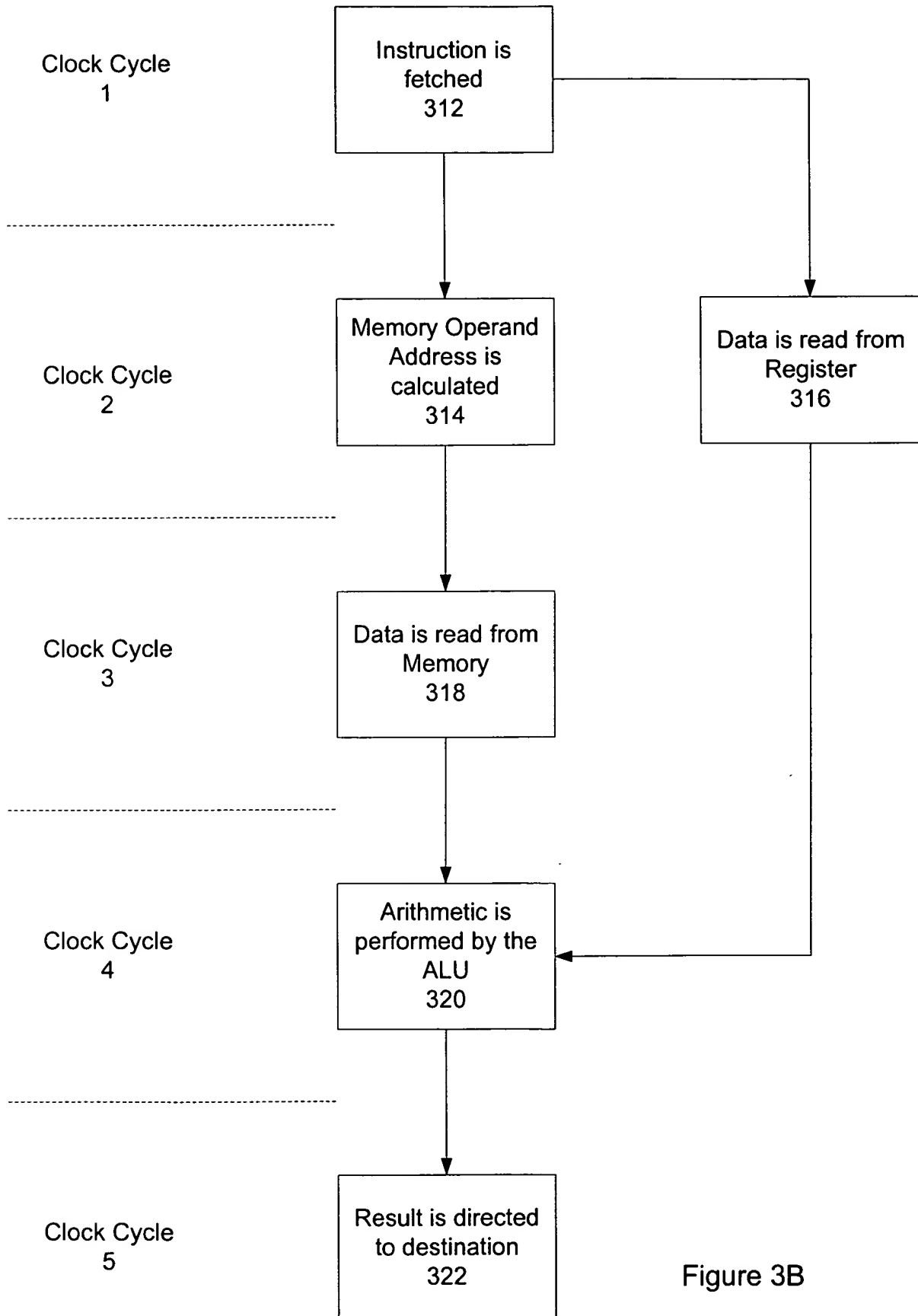


Figure 3B

400

OPCode 5 bits	Destination 11 bits	Source2 Register 5 bits	Source1 11 bits
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Figure 4

20880-06031-56288860

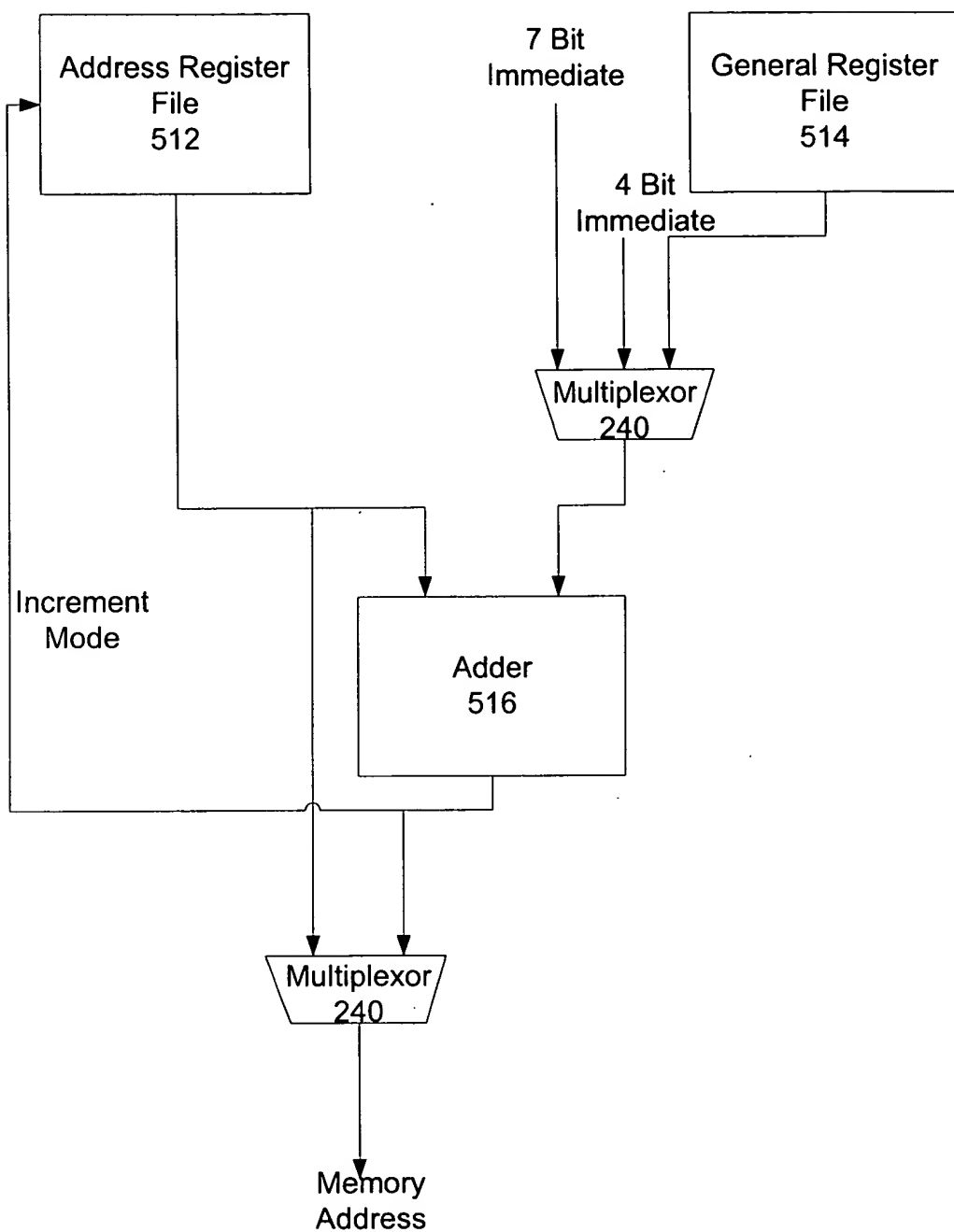


Figure 5



1	I <sub>6</sub>	I <sub>5</sub>	A <sub>2</sub> A <sub>1</sub> A <sub>0</sub>	I <sub>4</sub>	I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	Row 1
0	1	1		R <sub>4</sub>	R <sub>3</sub>	R <sub>2</sub>	R <sub>1</sub>	R <sub>0</sub>	Row 2
0	1	0		M	I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	Row 3
0	0	1	Register Direct						Row 4
0	0	0	Immediate						Row 5

Figure 6

2025-05-20 10:22:01

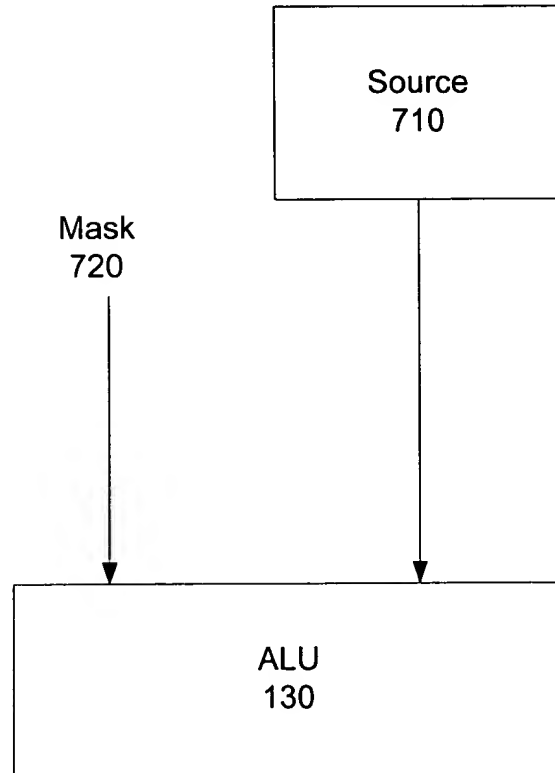


Figure 7

2022-09-05 10:56:50

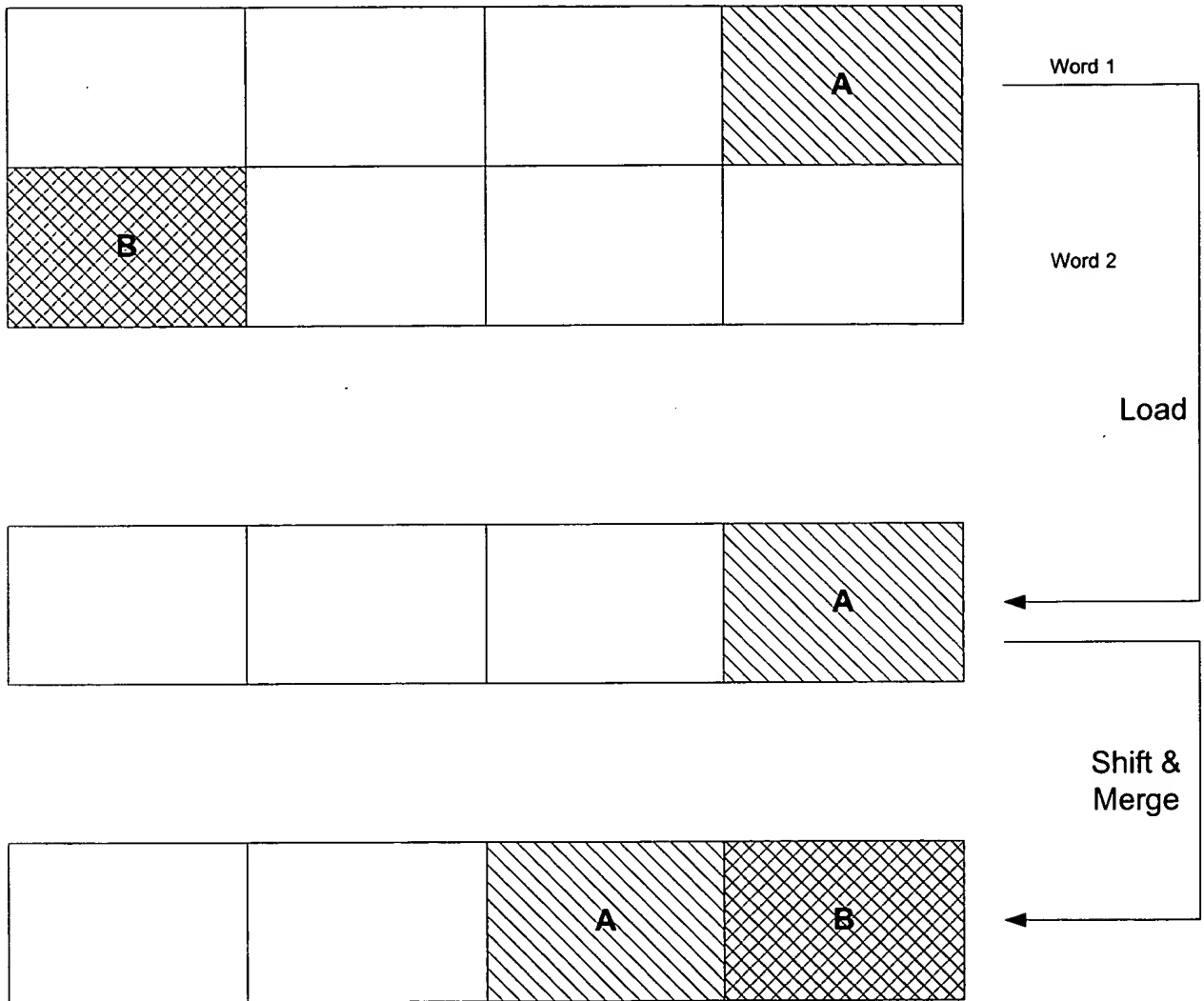


Figure 8

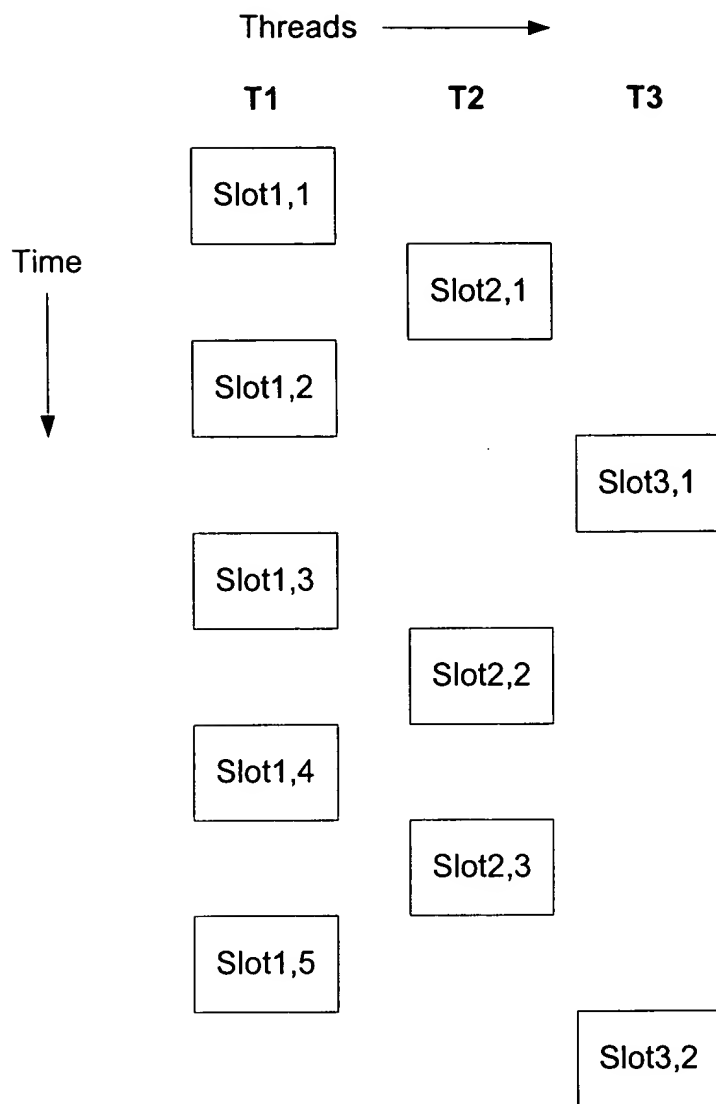


Figure 9